

METHOD OF FORMING TRENCH IN SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a method for manufacturing a semiconductor device, and more particularly, to a method for filling an insulation layer in a narrow trench of a small device while avoiding the formation of a void.

(b) Description of the Related Art

[0002] Shallow trench isolation (STI) is frequently used as an isolation structure in a semiconductor device. In STI, a trench is formed in a semiconductor substrate, and an insulation material is filled in the trench. Since the formation is limited to the size of the trench, which has as its object size a field region size, this configuration works favorably toward making the semiconductor device small.

[0003] It is important in STI to completely fill the trench with the insulation material without the formation of voids. US Patent Nos. 6,544,871, 4,528,047, 4,680,614, 6,180,490, 5,801,083, 6,524,931 are conventional techniques related to STI.

[0004] FIG. 1 shows a sectional view of a conventional STI structure. To form the conventional STI structure, a pad oxidation layer 2 is formed on a semiconductor substrate 1 to a thickness of approximately 200 Å. A silicon nitride layer 3 is then deposited on the pad oxidation layer 2, after which a photoresist layer is deposited on the silicon nitride layer 3. Next, the photoresist layer is exposed and developed such that an area thereof corresponding to where a trench is to be formed is removed. This results in the formation of a photoresist pattern (not shown).

[0005] Subsequently, using the photoresist pattern as a mask, the exposed portion of the silicon nitride layer 3, then the pad oxidation layer 2 and a predetermined section of the semiconductor substrate 1 (i.e., a section corresponding to a predetermined depth) under the removed section of the pad oxidation layer 2, are dry-
5 etched. A trench 100 is therefore formed in the semiconductor substrate 1. The photoresist pattern is removed after the formation of the trench 100, then a cleaning process is performed.

[0006] Subsequently, a liner oxidation layer 4 is formed over all exposed elements of the silicon nitride layer 3 and inner walls of the trench 100, after which a
10 trench oxidation layer 5 is thickly deposited on the liner oxidation layer 4 until at least the trench 100 is completely filled.

[0007] The liner oxidation layer 4 minimizes the stress transferred to the trench region during deposition of the trench oxidation layer 5. The liner oxidation layer 4 also prevents the uneven formation of the trench oxidation layer 5 caused by differences in
15 deposition speeds of the semiconductor substrate 1 and the silicon nitride layer 3. That is, the difference in the materials of the semiconductor substrate 1 and the silicon nitride layer 3 is such that their deposition speeds differ. In addition, with the formation of the liner oxidation layer 4, upper corner areas of the semiconductor substrate 1 adjacent to the trench 100 are rounded (i.e., prevented from being sharply pointed)
20 following a subsequent trench isolation process.

[0008] Next, chemical-mechanical polishing is performed on the trench oxidation layer 5 and the liner oxidation layer 4 until the silicon nitride layer 3 is exposed, that is, until the trench oxidation layer 5 and the liner oxidation layer 4 are flattened and flush with the silicon nitride layer 3. This completes the trench isolation process.

5 **[0009]** However, if an aspect ratio of the trench is increased by a reduction in trench width and an increase in trench depth in an attempt to increase the degree of integration of the device, there is a greater possibility of a void 6 being formed in the trench 100. That is, an entrance of the trench 100 may be partially blocked before a deep area thereof is filled during deposition of the trench oxidation layer 5. The
10 formation of a void 6, therefore, prevents the trench 100 from being completely filled.

[0010] Using present trench filling techniques, the formation of voids may be avoided with trenches of a width of $0.24\mu\text{ m}$ or greater. However, any reduction in the width to, for example, $0.21\mu\text{ m}$ or $0.18\mu\text{ m}$ results in the formation of voids.

[0011] The formation of a void 6 in the trench oxidation layer 5 as described
15 above may result in the void 6 being exposed following chemical-mechanical polishing to flatten the trench oxidation layer 5. If this occurs, polysilicon deposited to form an electrode in a subsequent process enters the void 6 such that leakage current develops. This results in severe malfunctioning of the device.

SUMMARY OF THE INVENTION

20 **[0012]** In one exemplary embodiment of the present invention, there is provided

a method for forming a trench oxidation layer to completely fill a trench while avoiding the formation of a void.

[0013] In an exemplary embodiment of the present invention, a method of forming a trench in a semiconductor device includes forming a polish stop layer on a semiconductor substrate. The polish stop layer and the semiconductor substrate are then etched to form a trench. The semiconductor substrate is etched to a predetermined depth. Also, etching is performed such that ends of the polish stop layer adjacent to the trench are rounded. Next, an insulation layer that fills the trench is formed.

[0014] Etching is performed such that following the injection of CHF_3 , CF_4 , O_2 , HeO_2 , or Ar, plasma is created and dry etching is performed. That is, at most 60sccm of CHF_3 gas, at most 60sccm of CF_4 gas, at most 30sccm of O_2 gas, at most 60sccm of HeO_2 gas, or at most 200sccm of Ar gas is injected. 50-500W of power is applied to generate plasma in a state where CHF_3 , CF_4 , O_2 , HeO_2 , or Ar is injected. Further, a pressure environment of 5-100mTorr is created for use during etching.

[0015] Prior to forming a polish stop layer on a semiconductor substrate, an anti-reflection coating is formed on the polish stop layer, and the anti-reflection coating is selectively etched to form an anti-reflection coating pattern. An area of the polish stop layer exposed through the anti-reflection coating pattern and the semiconductor substrate to a predetermined depth are etched to form the trench, and ends of the anti-

reflection coating pattern and ends of the polish stop layer under the ends of the anti-reflection coating pattern are etched such that the ends of the anti-reflection coating are formed into a rounded configuration.

[0016] The polish stop layer is deposited to a thickness of 1000-3000 Å. Further, the polish stop layer is made of a material that is more slowly polished than insulation material of the insulation layer. As an example, the polish stop layer is formed of a silicon nitride layer deposited to a thickness of 1000-3000 Å.

[0017] During forming an insulation layer that fills the trench, following the formation of the insulation layer to cover the polish stop layer and inner walls of the trench, chemical-mechanical polishing is performed on the insulation layer until the polish stop layer is exposed.

[0018] In addition, prior to forming the insulation layer, a liner oxidation layer is formed on the polish stop layer and the trench, then the insulation layer is formed on the liner oxidation layer such that the trench is filled with a material forming the insulation layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings, which together with the specification, illustrate an exemplary embodiment of the present invention, and, together with the description, serve to explain the principles of the present invention.

[0020] FIG. 1 is a sectional view of a conventional shallow trench isolation

structure.

[0021] FIGS. 2a through 2d are sectional views used to describe a method for forming a trench in a semiconductor device according to an exemplary embodiment of the present invention.

5 **DETAILED DESCRIPTION**

[0022] An exemplary embodiment of the present invention will now be described in detail with reference to the accompanying drawings.

[0023] FIGS. 2a through 2d are sectional views used to describe a method for forming a trench in a semiconductor device according to an exemplary embodiment of the present invention.

10 **[0024]** With reference first to FIG. 2a, a pad oxidation layer 12 is thinly deposited on a semiconductor substrate 11. Next, a silicon nitride layer 13 is deposited on the pad oxidation layer 12, then an anti-reflection coating (ARC) 14 is deposited on the silicon nitride layer 13.

15 **[0025]** The pad oxidation layer 12 is selectively deposited to minimize stress of the silicon nitride layer 13 from being transmitted to the semiconductor substrate 11. Preferably, the pad oxidation layer 12 is deposited thinly at a thickness of 100-300 Å. It is to be noted that the formation of the pad oxidation layer 12 is optional.

20 **[0026]** The silicon nitride layer 13 is used as a polish stop layer in a subsequent process of performing chemical-mechanical polishing of a trench oxidation layer.

However, the present invention is not limited to the silicon nitride of the silicon nitride layer 13 and it is possible to use a material that is polished more slowly than an insulation material that fills a trench. It is preferable that the polish stop layer (i.e., the silicon nitride layer 13) be formed to a thickness of 1000-3000 Å. As an example, the silicon nitride layer 13 may be formed to a thickness of 2000 Å.

[0027] The ARC 14 is used to more efficiently enable etching for rounding a silicon nitride layer pattern. The ARC 14 is not limited to any particular material and it is possible to use any conventional ARC made of an organic material.

[0028] Following the formation of the ARC 14, a photosensitive layer is deposited thereon, then the photoresist layer is exposed such that a section thereof where a trench is to be formed is removed. A photoresist pattern 15 is formed from this process.

[0029] Subsequently, with reference to FIG. 2b, the photoresist pattern is used as a mask to etch an exposed area of the ARC 14.

[0030] With reference to FIG. 2c, an exposed portion of the silicon nitride film 13, then the pad oxidation layer 12 and a predetermined section of the semiconductor substrate 11 (i.e., a section corresponding to a predetermined depth) under the removed section of the ARC 14 are dry-etched to thereby form a trench 100. Next, the photoresist pattern 15 and the ARC 14 are removed, then a cleaning process is performed.

[0031] During dry etching to form the trench 100, etching conditions are

controlled such that a small amount of exposed ends of the ARC 14 is removed and upper corners of the silicon nitride layer 13 thereunder are rounded. That is, the amount of the etching gas is varied depending on which type of element or compound is used for the etching gas. For example, to realize this configuration of the ARC 14 and the silicon nitride layer 13, there is used 60sccm or less of CHF_3 gas, 50sccm or less of CF_4 gas, 30sccm or less of O_2 gas, 60sccm or less of HeO_2 gas, or 200sccm or less of Ar gas.

[0032] Further, in a state where the above etching gas is being injected, dry etching is performed with the application of power for creating plasma in the range of 50-500W, and in a pressurized environment of 5-100mTorr.

[0033] If dry etching is performed under these conditions, a sidewall polymer formed in the initial stages of etching the silicon nitride layer 13 is removed such that the ends of the ARC 14 are etched. As a result, areas of the silicon nitride layer 13 under the ends of the ARC 14 are etched such that the upper corners are rounded. This acts to increase an opening size of the trench 100.

[0034] Subsequently, with reference to FIG. 2d, a liner oxidation layer 16 is deposited over all exposed elements including the silicon nitride layer 13, exposed ends of the pad oxidation layer 12, and inner walls of the trench 100 formed by the semiconductor substrate 11. An oxidation layer 17 is then thickly deposited on the liner oxidation layer 16 until sufficiently filling the trench 100.

[0035] Since the upper corners of the silicon nitride layer 13 are rounded, the opening of the trench 100 is enlarged to thereby prevent the blocking of the opening before a deep portion of the trench 100 is filled. As a result, the oxidation layer 17 may be formed such that the inside of the trench 100 is completely filled without the formation of a void therein.

[0036] Next, chemical-mechanical polishing is performed on the oxidation layer 17 then on the liner oxidation layer 16 thereunder until the silicon nitride layer 13 is exposed. That is, chemical-mechanical polishing is performed until the oxidation layer 17 and the liner oxidation layer 16 that are above the silicon nitride layer 13 are removed such that these elements are flattened and made flush with the silicon nitride layer 13. This completes the shallow trench isolation process.

[0037] In the present invention described above, following the formation of the ARC on the silicon nitride layer, etching conditions for the formation of the trench are controlled such that ends of the ARC are etched and the silicon nitride layer thereunder is also etched. As a result, upper corners of the silicon nitride layer are rounded such that the trench oxidation layer may be formed without the formation of a void in the trench. This acts to prevent a reduction in device reliability resulting from current leakage, which occurs with the formation of a void, and also to improve device yield is improved.

[0038] Although an embodiment of the present invention has been described in

Docket No. OPP 031050 US
Express Mail No. ER085424762US

detail hereinabove in connection with certain exemplary embodiments, it should be understood that the invention is not limited to the disclosed exemplary embodiment, but, on the contrary is intended to cover various modifications and/or equivalent arrangements included within the spirit and scope of the present invention, as defined in the appended claims.